200-mA, Low-I_Q, Low-Dropout Regulator for Portable Devices

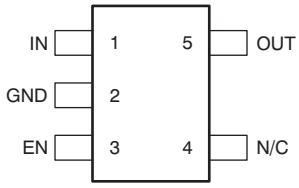
FEATURES

- **Very Low Dropout:**
  - **43 mV at I_{OUT} = 50 mA, V_{OUT} = 2.8 V**
  - **85 mV at I_{OUT} = 100 mA, V_{OUT} = 2.8 V**
  - **175 mV at I_{OUT} = 200 mA, V_{OUT} = 2.35 V**
- **2% Accuracy**
- **Low I_Q: 31 μA**
- **Available in Fixed-Output Voltages from 0.7 V to 4.8 V**
- **High PSRR: 68 dB at 1 kHz**
- **Stable with Effective Capacitance of 0.1 μF**
- **Thermal Shutdown and Overcurrent Protection**
- **Available in 1,5-mm × 1,5-mm SON-6, SOT23-5, and SC-70 packages**

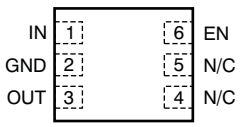
APPLICATIONS

- **Wireless Handsets**
- **Smart Phones, PDAs**
- **MP3 Players**
- **ZigBee® Networks**
- **Bluetooth® Devices**
- **Li-Ion Operated Handheld Products**
- **WLAN and Other PC Add-on Cards**

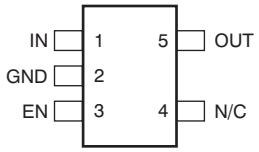
TLV700xxDDC
TSOT23-5
(TOP VIEW)



TLV700xx DSE
1,5-mm x 1,5-mm SON
(TOP VIEW)



TLV700xx DCK
SC70-5 PACKAGE
(TOP VIEW)

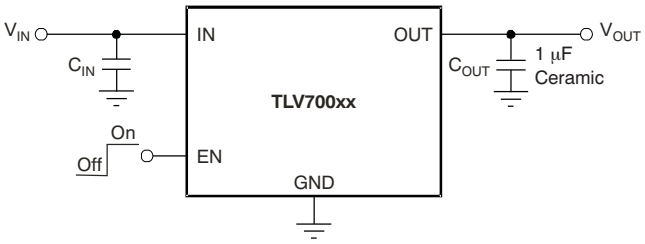


DESCRIPTION

The TLV700xx/TLV701xx series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage make this series of devices ideal for most battery-operated handheld equipment. All device versions have thermal shutdown and current limit for safety.

Furthermore, these devices are stable with an effective output capacitance of only 0.1 μF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

The TLV700xx series of LDOs are available in 1,5-mm x 1,5-mm SON-6, TSOT23-5, and SC-70 packages. The TLV701xx series of LDOs are available in a 1,5-mm x 1,5-mm SON-6 package.



Typical Application Circuit (Fixed-Voltage Versions)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT} (2)
TLV700**xx** ***yyy z*** TLV701**xx** ***yyy z***	**XX** is nominal output voltage (for example, 28 = 2.8 V). **YYY** is the package designator. **Z** is tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 0.7 V to 4.8 V in 50-mV increments are available. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to +125°C (unless otherwise noted). All voltages are with respect to GND.

PARAMETER		TLV700xx/TLV701xx	UNIT
Input voltage range, V_{IN}		–0.3 to +6.0	V
Enable voltage range, V_{EN}		–0.3 to +6.0	V
Output voltage range, V_{OUT}		–0.3 to +6.0	V
Maximum output current, I_{OUT}		Internally limited	
Output short-circuit duration		Indefinite	
Total continuous power dissipation, P_{DISS}		See Dissipation Ratings Table	
ESD rating	Human body model (HBM)	2	kV
	Charged device model (CDM)	500	V
Operating junction temperature range, T_J		–55 to +150	°C
Storage temperature range, T_{STG}		–55 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C	T_A = +70°C	T_A = +85°C
Low-K(1)	DCK	165°C/W	395°C/W	2.5 mW/°C	250 mW	140 mW	100 mW
High-K(2)	DCK	165°C/W	315°C/W	3.2 mW/°C	320 mW	175 mW	130 mW
High-K(2)	DSE	67°C/W	180°C/W	4.55 mW/°C	555 mW	305 mW	222 mW
Low-K(1)	DDC	90°C/W	280°C/W	3.6 mW/°C	360 mW	200 mW	145 mW
High-K(2)	DDC	90°C/W	200°C/W	5.0 mW/°C	500 mW	275 mW	200 mW

(1) The JEDEC low-K (1s) board used to derive this data was a 3-inch × 3-inch, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3-inch × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

At $V_{IN} = V_{OUT(Typ)} + 0.3$ V or 2.0 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1.0 μF, and T_J = –40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			2.0		5.5	V
V_{OUT}	DC output accuracy	–40°C ≤ T_J ≤ +125°C	V_{OUT} ≥ 1 V	–2		+2	%
			V_{OUT} < 1 V	–20		+20	mV
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA			1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 200 mA			1	15	mV
V_{DO}	Dropout voltage[1]	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 50 mA, V_{OUT} = 2.8 V			43		mV
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 100 mA, V_{OUT} = 2.8 V			85		mV
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 200 mA, V_{OUT} = 2.35 V			175	250	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$		220	350	550	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA			31	55	μA
		I_{OUT} = 200 mA, V_{IN} = V_{OUT} + 0.5 V			270		μA
I_{SHDN}	Ground pin current (shutdown)	V_{EN} ≤ 0.4 V, V_{IN} = 2.0 V			400		nA
		V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 4.5 V			1	2	μA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, f = 1 kHz			68		dB
V_N	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			48		μV_{RMS}
t_{STR}	Startup time[2]	C_{OUT} = 1.0 μF, I_{OUT} = 200 mA			100		μs
$V_{EN(HI)}$	Enable pin high (enabled)			0.9		V_{IN}	V
$V_{EN(LO)}$	Enable pin low (disabled)			0		0.4	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 5.5 V			0.04	0.5	μA
UVLO	Undervoltage lockout	V_{IN} rising			1.9		V
$R_{DISCHARGE}$	Active pulldown resistance (TLV701xx only)	V_{EN} = 0 V			120		Ω
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			+160		°C
		Reset, temperature decreasing			+140		°C
T_J	Operating junction temperature			–40		+125	°C

(1) V_{DO} is measured for devices with $V_{OUT(NOM)}$ ≥ 2.35 V.
(2) Startup time = time from EN assertion to 0.98 × $V_{OUT(NOM)}$.

FUNCTIONAL BLOCK DIAGRAMS

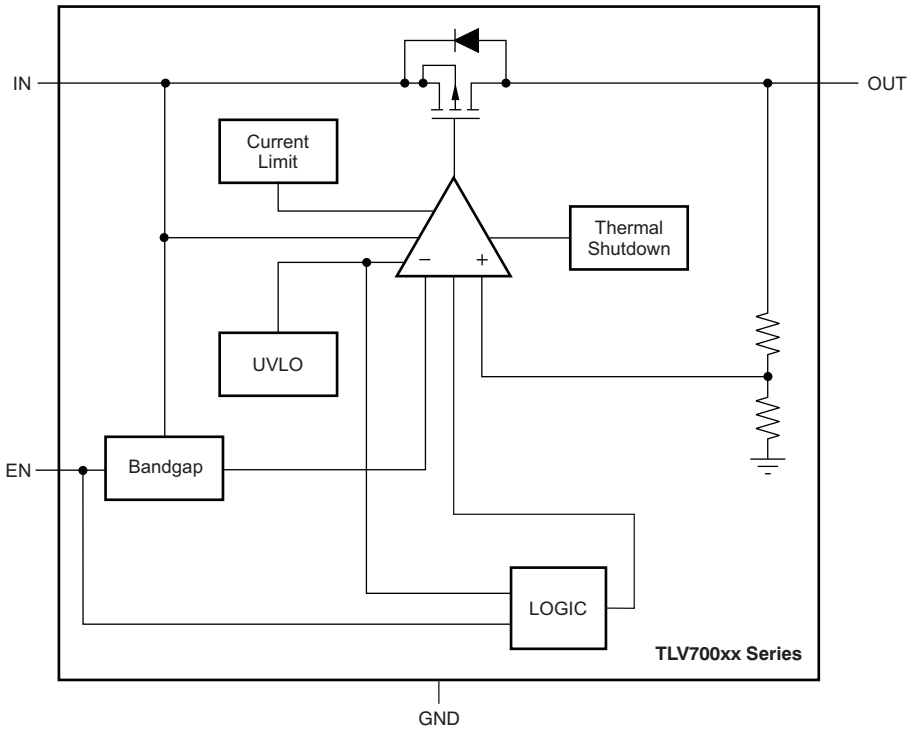


Figure 1. TLV700xx

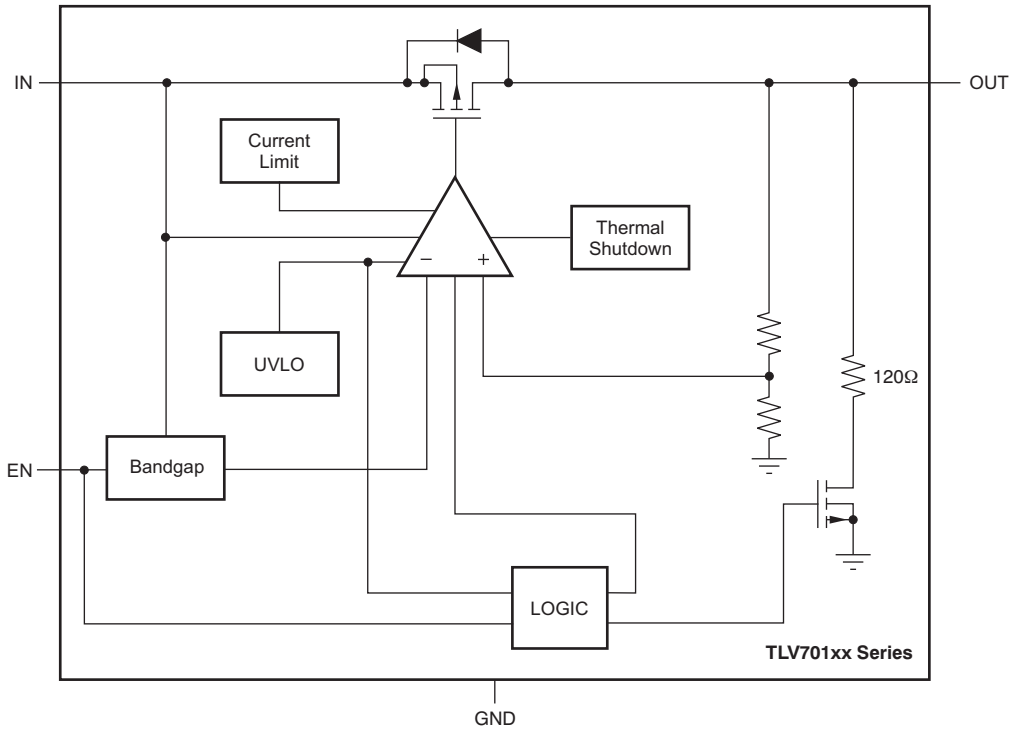
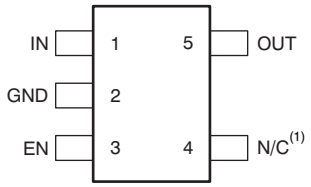


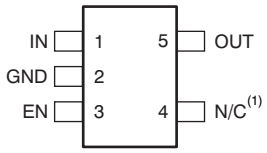
Figure 2. TLV701xx

PIN CONFIGURATIONS

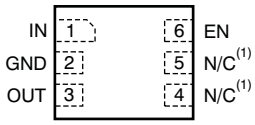
DDC PACKAGE
TSOT23-5
(TOP VIEW)



DCK PACKAGE
SC70-5
(TOP VIEW)



DSE PACKAGE
SON-6
(TOP VIEW)



(1) No connection.

PIN DESCRIPTIONS

NAME	SON-6 DSE	SC70-5 DCK	TSOT23-5 DDC	DESCRIPTION
IN	1	1	1	Input pin. A small 1-μF ceramic capacitor is recommended from this pin to ground to assure stability and good transient performance. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
GND	2	2	2	Ground pin
EN	6	3	3	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode and reduces operating current to 1 μA, nominal. For TLV701xx, output voltage is discharged through an internal 120-Ω resistor when device is shut down.
NC	4, 5	4	4	No connection. This pin can be tied to ground to improve thermal dissipation.
OUT	3	5	5	Regulated output voltage pin. A small 1-μF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = +25°C.

TLV70018
LINE REGULATION

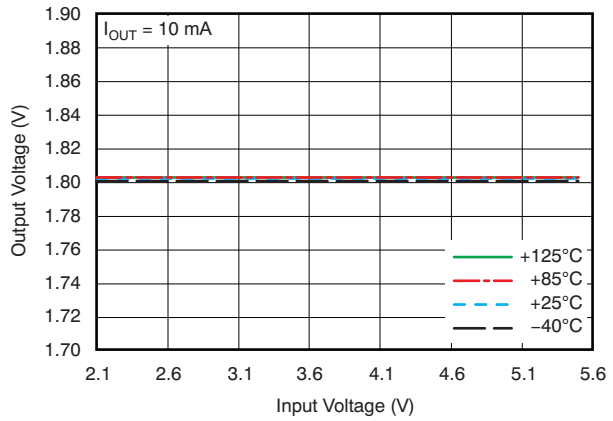


Figure 3.

TLV70018
LINE REGULATION

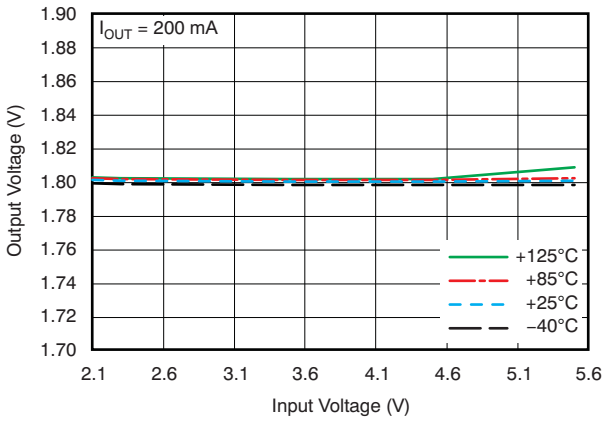


Figure 4.

TLV70018
LOAD REGULATION

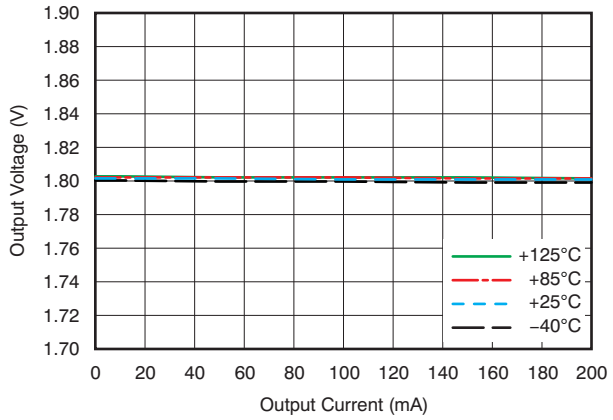


Figure 5.

DROPOUT VOLTAGE vs INPUT VOLTAGE
V_{OUT} = 4.8V

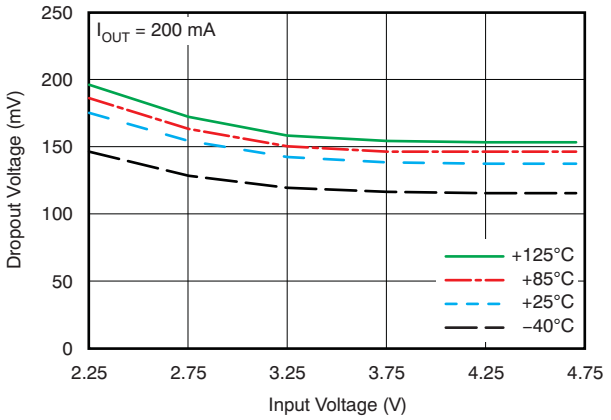


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = +25°C.

TLV70048
DROPOUT VOLTAGE vs OUTPUT CURRENT

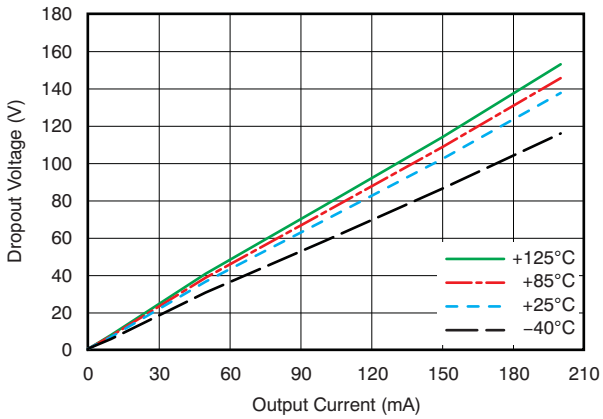


Figure 7.

TLV70018
OUTPUT VOLTAGE vs TEMPERATURE

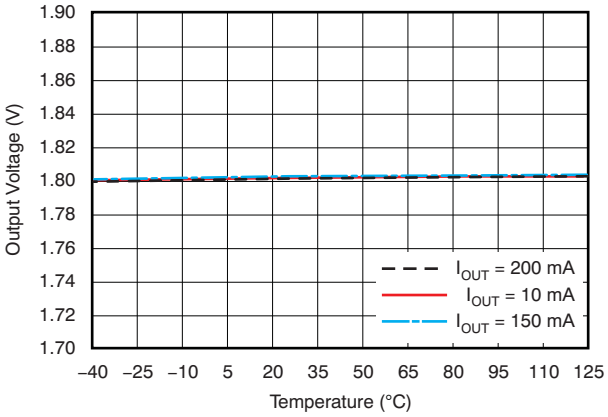


Figure 8.

TLV70018
GROUND PIN CURRENT vs INPUT VOLTAGE

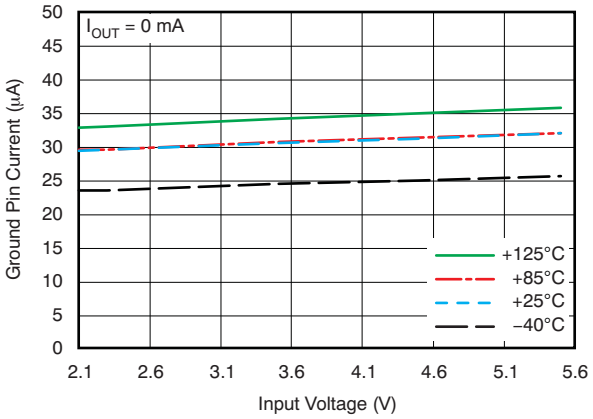


Figure 9.

TLV70018
GROUND PIN CURRENT vs LOAD

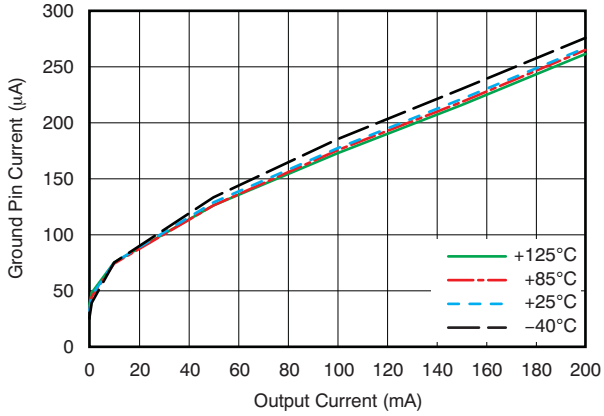


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = +25°C.

TLV70018
GROUND PIN CURRENT vs TEMPERATURE

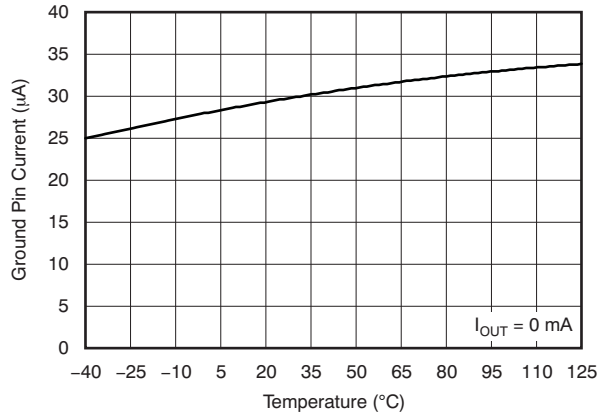


Figure 11.

TLV70018
SHUTDOWN CURRENT vs INPUT VOLTAGE

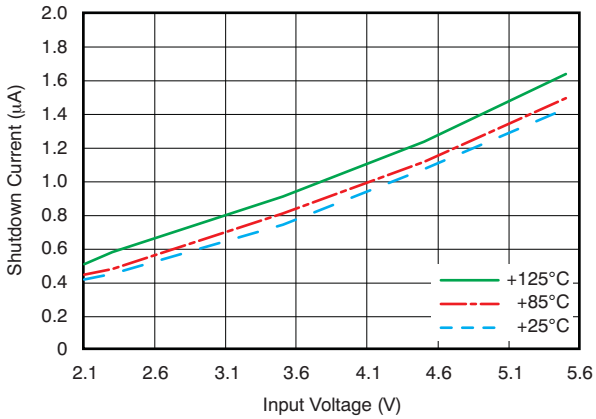


Figure 12.

TLV70018
CURRENT LIMIT vs INPUT VOLTAGE

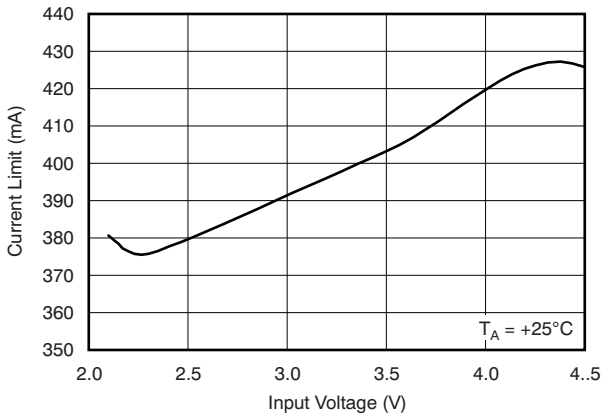


Figure 13.

TLV70018
POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

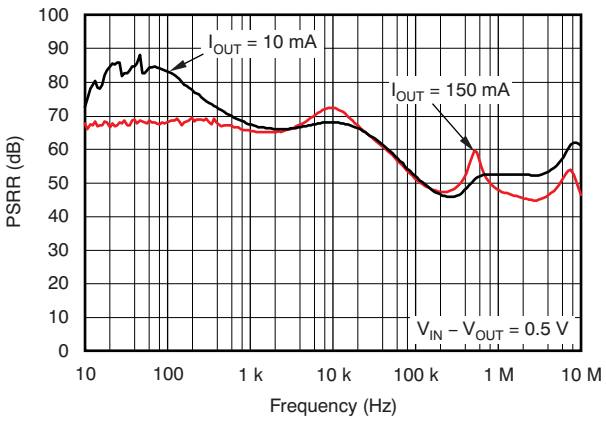


Figure 14.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = +25°C.

TLV70018
POWER-SUPPLY RIPPLE REJECTION vs INPUT VOLTAGE

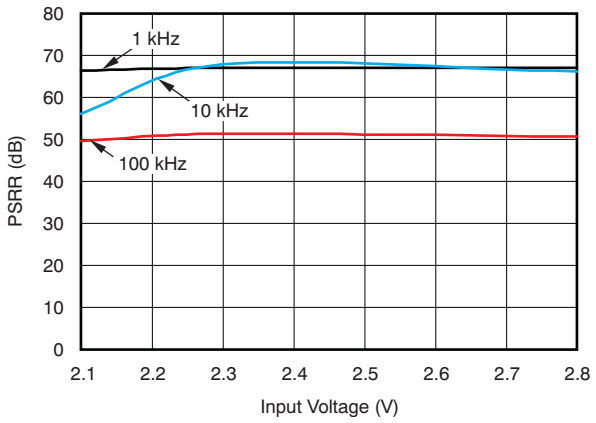


Figure 15.

TLV70018
OUTPUT SPECTRAL NOISE DENSITY vs OUTPUT VOLTAGE

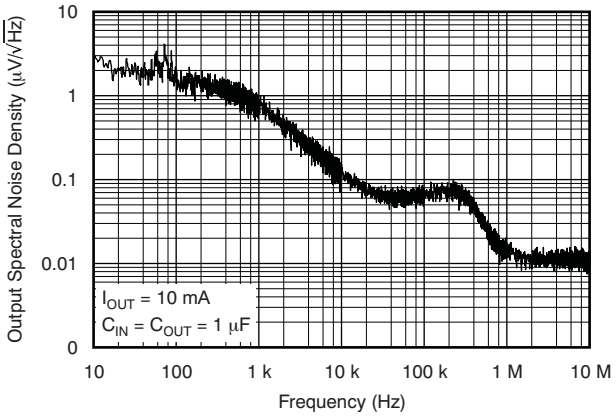


Figure 16.

TLV70018
LOAD TRANSIENT RESPONSE

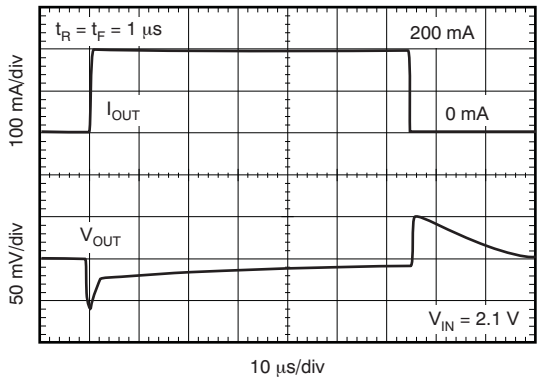


Figure 17.

TLV70018
LOAD TRANSIENT RESPONSE

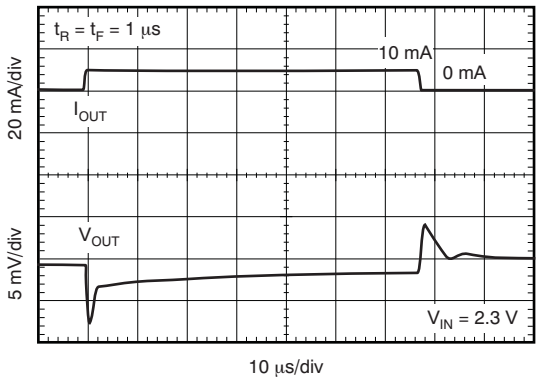


Figure 18.

TLV70018
LOAD TRANSIENT RESPONSE

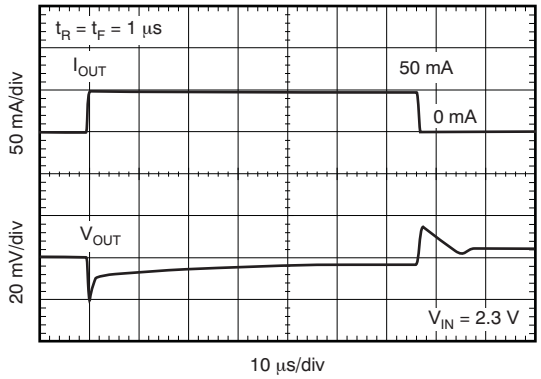


Figure 19.

TLV70018
LINE TRANSIENT RESPONSE

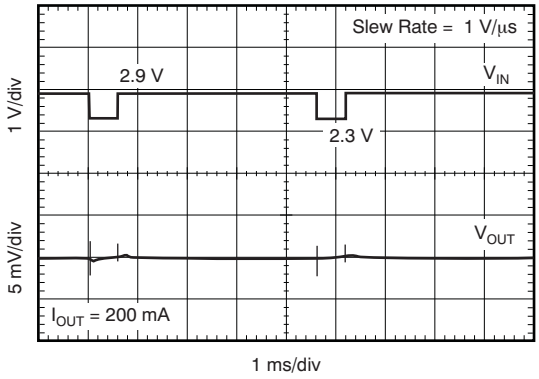


Figure 20.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = +25°C.

TLV70018
LINE TRANSIENT RESPONSE

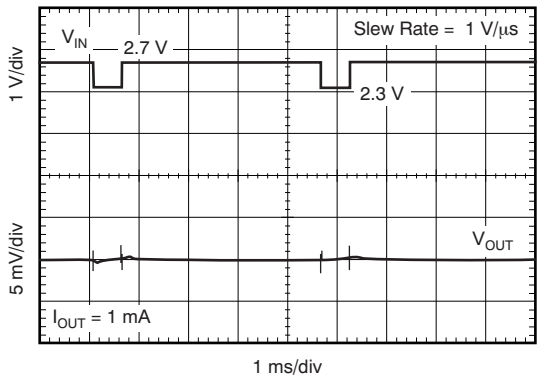


Figure 21.

TLV70018
LINE TRANSIENT RESPONSE

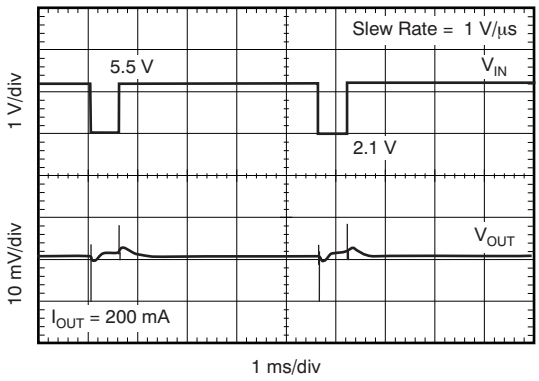


Figure 22.

TLV70018
V_{IN} RAMP UP, RAMP DOWN RESPONSE

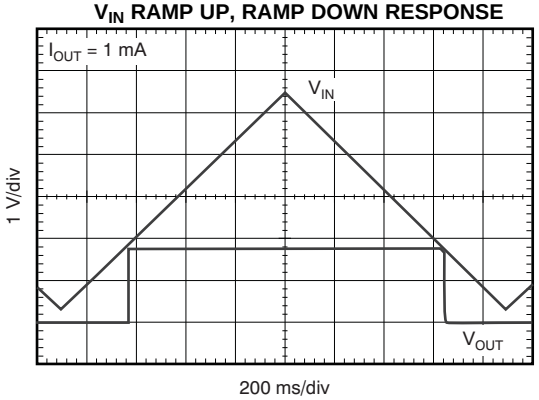


Figure 23.

APPLICATION INFORMATION

The TLV700xx/TLV701xx belong to a new family of next-generation value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for RF portable applications. This family of regulators offers sub-bandgap output voltages down to 0.7 V, current limit, and thermal protection, and is specified from –40°C to +125°C.

Input and Output Capacitor Requirements

1.0-μF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV700xx/TLV701xx are designed to be stable with an *effective capacitance* of 0.1 μF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 μF. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with 0.1-μF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

Note that using a 0.1-μF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions would be less than 0.1 μF. Maximum ESR should be less than 200 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-μF to 1.0-μF, low ESR capacitor across the IN pin and GND in of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-μF input capacitor may be necessary to ensure stability.

Board Layout Recommendations to Improve PSRR and Noise Performance

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR performance.

Internal Current Limit

The TLV700xx/TLV701xx internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates (V_{IN} – V_{OUT}) × I_{LIMIT} until thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the Thermal Information section for more details.

The PMOS pass element in the TLV700xx/TLV701xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at EN pin goes above 0.9V. This relatively lower value of voltage required to turn the LDO on can be exploited to power the LDO with a GPIO of recent processors whose GPIO Logic 1 voltage level is lower than traditional microcontrollers. The device is turned OFF when the EN pin is held at less than 0.4V. When shutdown capability is not required, EN can be connected to the IN pin.

The TLV701 has an internal active pull-down circuitry that discharges the output with a time constant of:

$$\tau = \frac{(120 \bullet R_L)}{(120 + R_L)} \bullet C_{OUT} \quad (1)$$

with:

- R_L = Load resistance
- C_{OUT} = Output capacitor

Dropout Voltage

The TLV700xx/TLV701xx use a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage ($V_{DO)}$, the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 15 in the Typical Characteristics section.

Transient Response

As with any regulator, increasing the size of the output capacitor reduces over-/undershoot magnitude but increases the duration of the transient response.

Undervoltage Lockout (UVLO)

The TLV700xx/TLV701xx use an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly.

Thermal Information

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV700xx/TLV701xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV700xx/TLV701xx into thermal shutdown degrades device reliability.

Power Dissipation

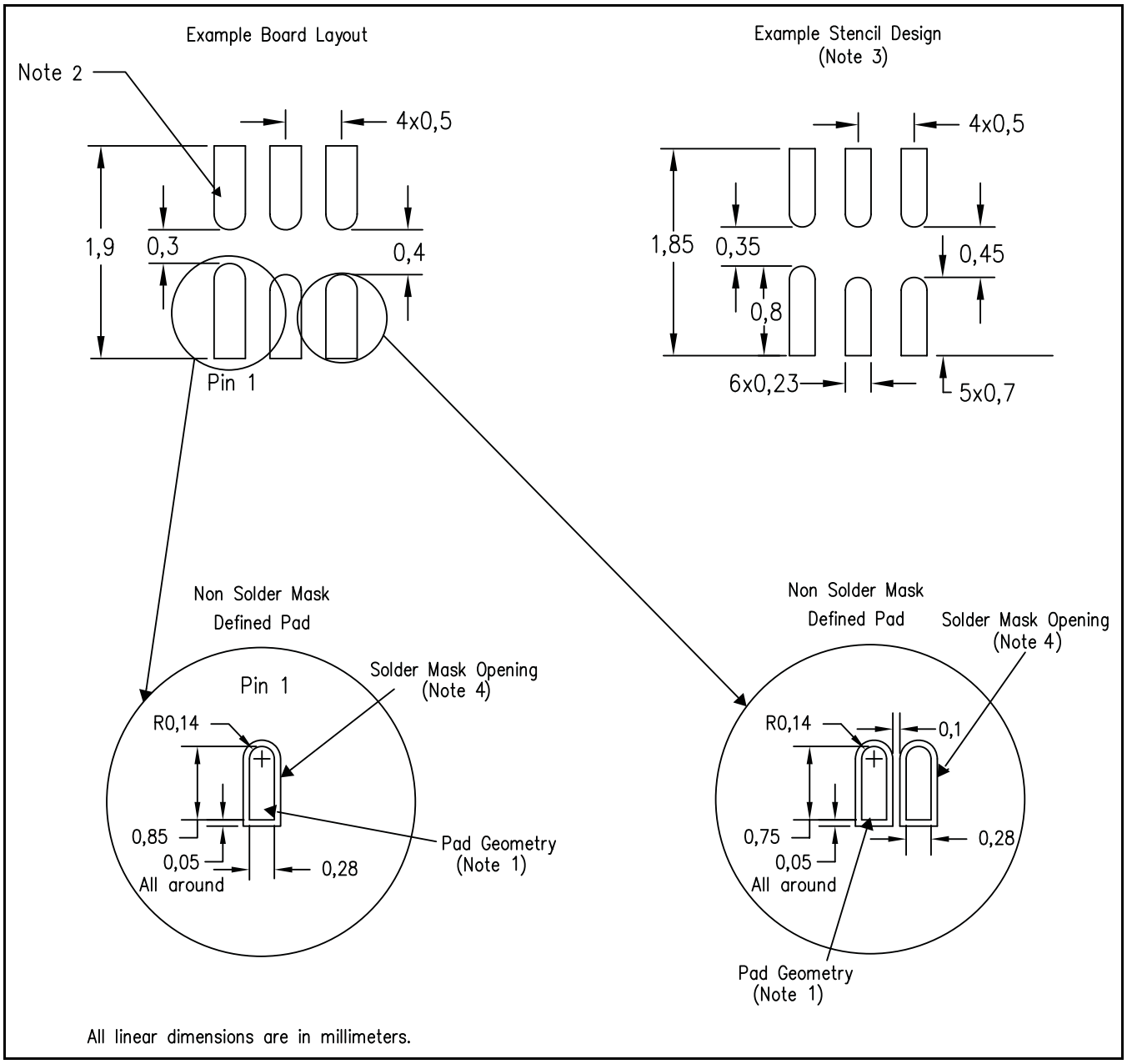
The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low and high-K boards are given in the Dissipation Ratings table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 2.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Package Mounting

Solder pad footprint recommendations for the TLV700xx/TLV701xx are available from the Texas Instruments web site at www.ti.com. The recommended land patterns for the DSE, DDC, and DCK packages are shown in Figure 24, Figure 25, and Figure 26, respectively. Figure 27, Figure 28, and Figure 29 show the mechanical package dimensions for the DSE, DDC, and DCK packages, respectively.



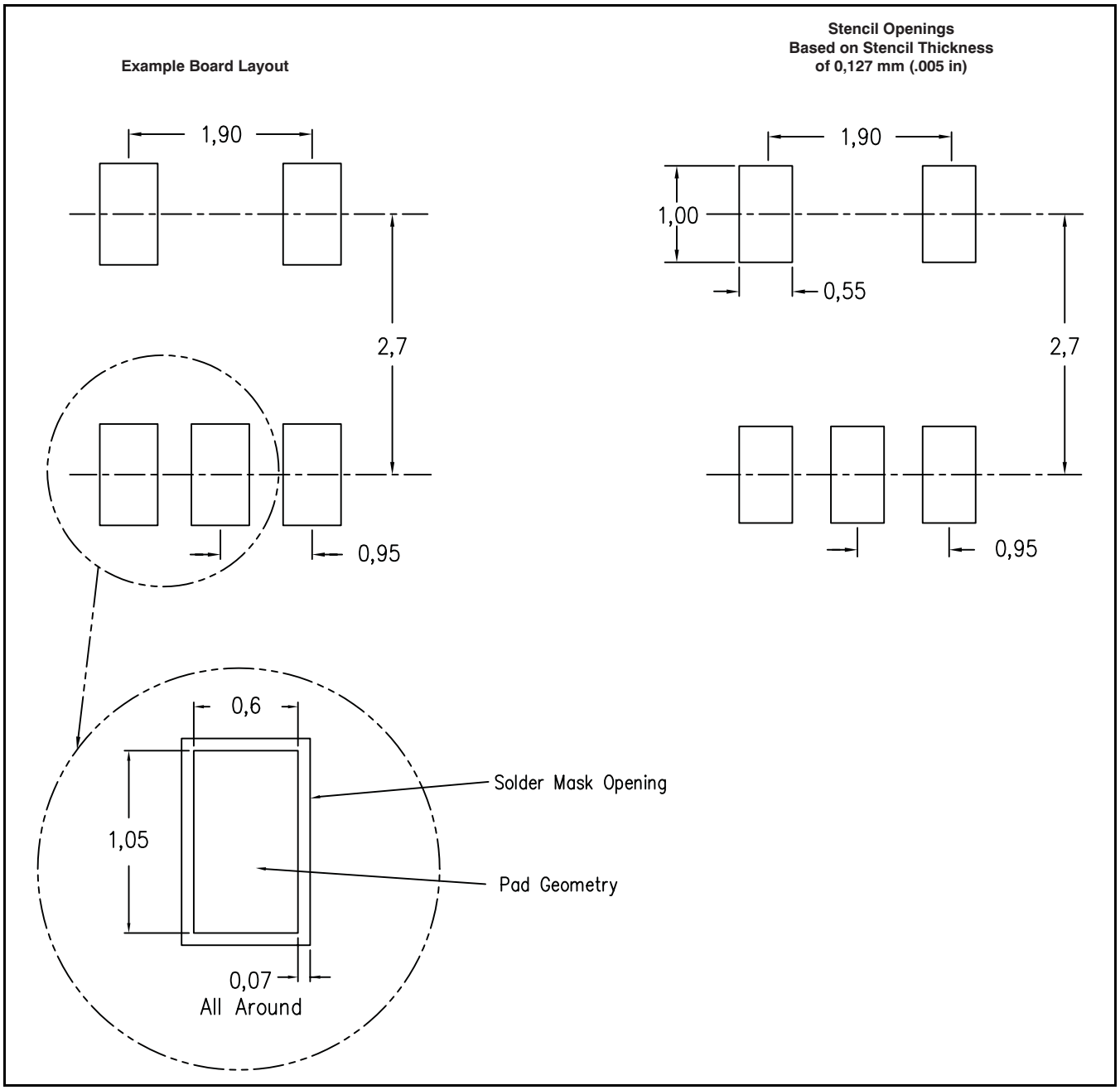
(1) Publication IPC-7351 is recommended for alternate designs.

(2) For more information, refer to TI application notes SCBA017 and SLUA271 (*Quad Flatpack No-Lead Logic Packages* and *QFN/SON PCB Attachment*, respectively) for specific thermal information, via requirements, and additional recommendations for board layout. These documents are available at the Texas Instruments web site (http://www.ti.com) by searching for the literature number.

(3) Laser-cutting apertures with trapedzoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for stencil design considerations.

(4) Customers should contact their board fabrication site for minimum solder mask tolerances between signal pads.

Figure 24. Recommended Land Pattern for DSE Package



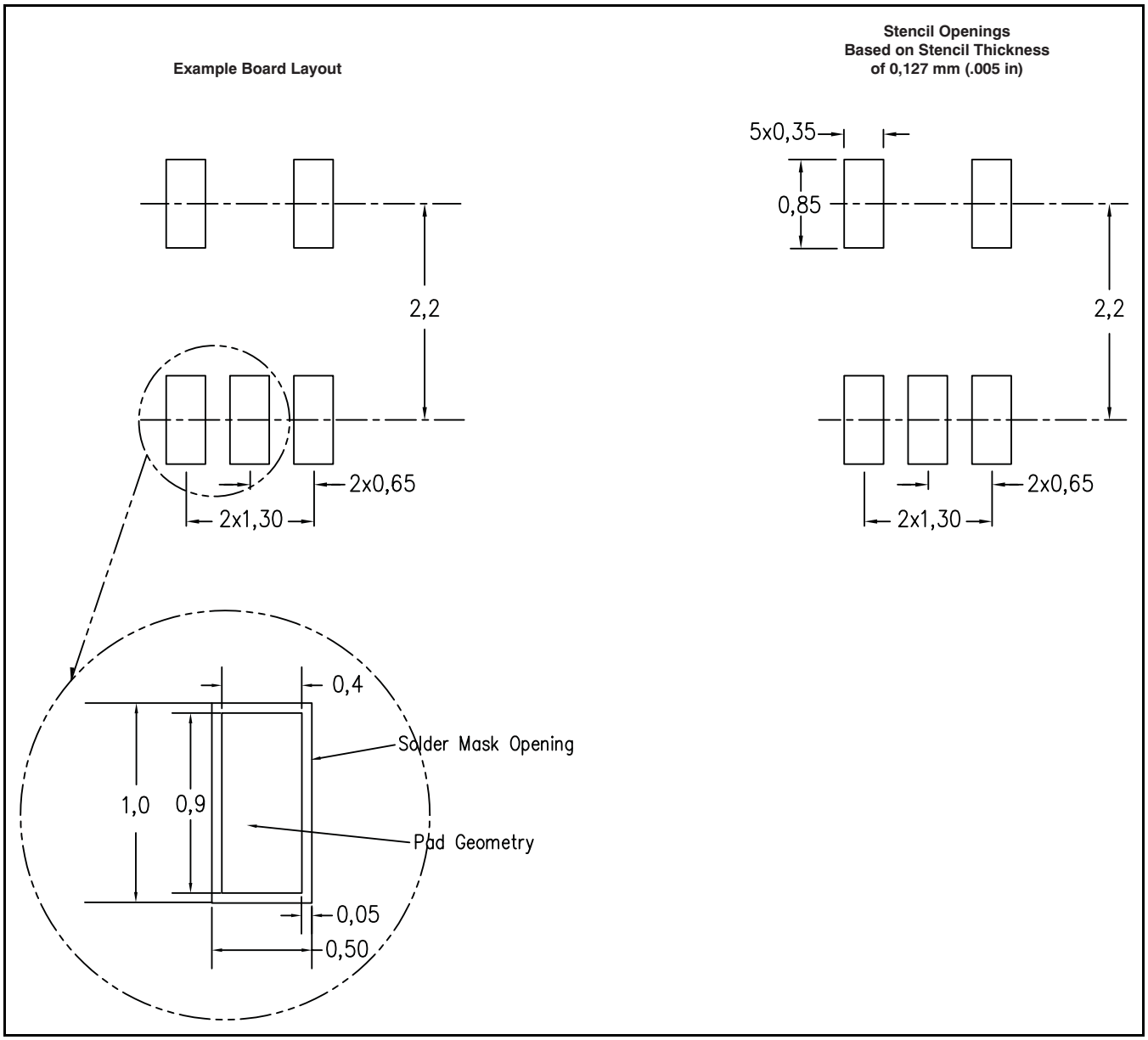
(1) All linear dimensions are in millimeters.

(2) Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.

(3) Publication IPC-7351 is recommended for alternate designs.

(4) Laser-cutting apertures with trapedzoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric load solder paste. Refer to IPC-7525 for other stencil recommendations.

Figure 25. Recommended Land Pattern for DDC Package



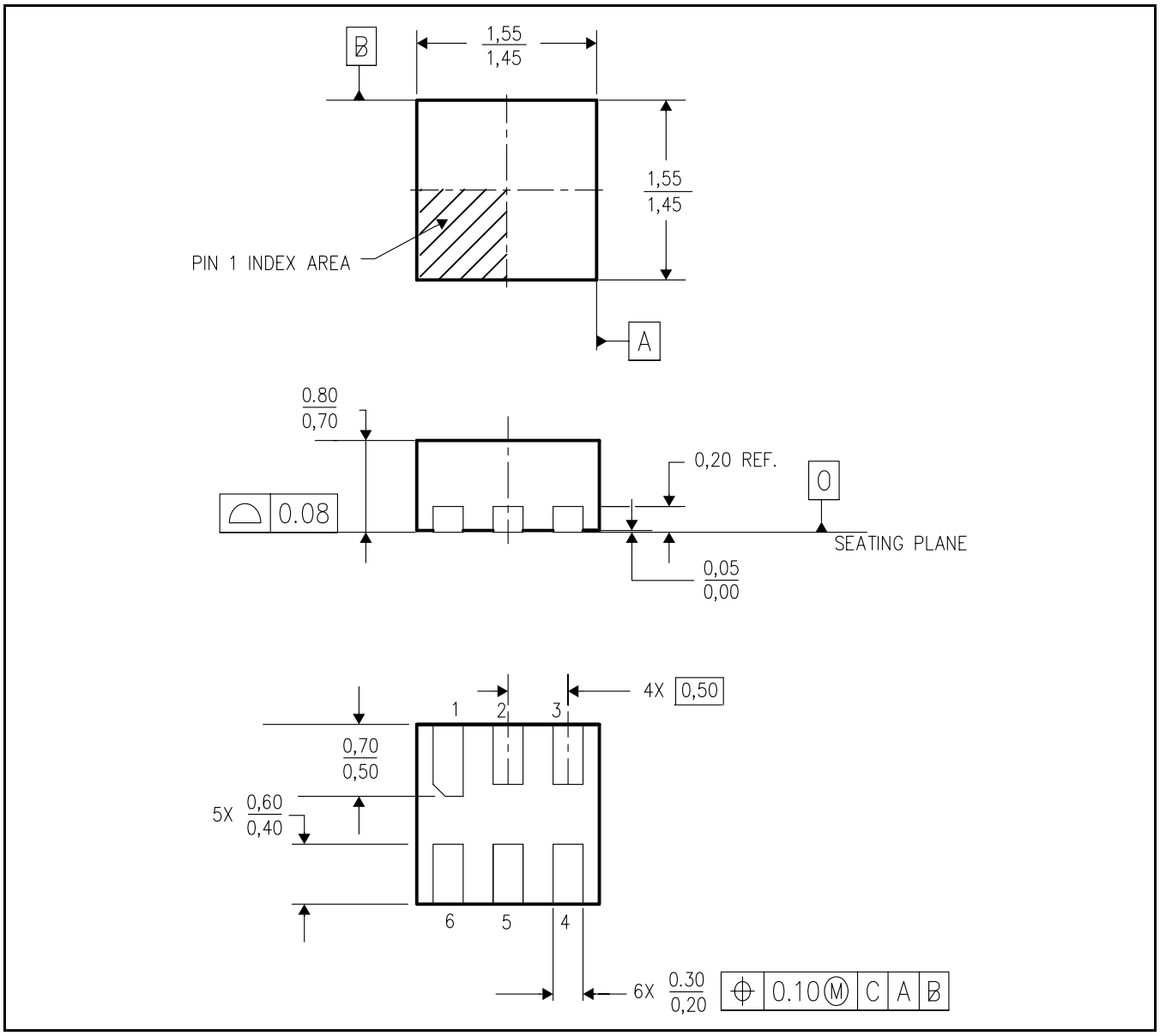
(1) All linear dimensions are in millimeters.

(2) Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.

(3) Publication IPC-7351 is recommended for alternate designs.

(4) Laser-cutting apertures with trapedzoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric load solder paste. Refer to IPC-7525 for other stencil recommendations.

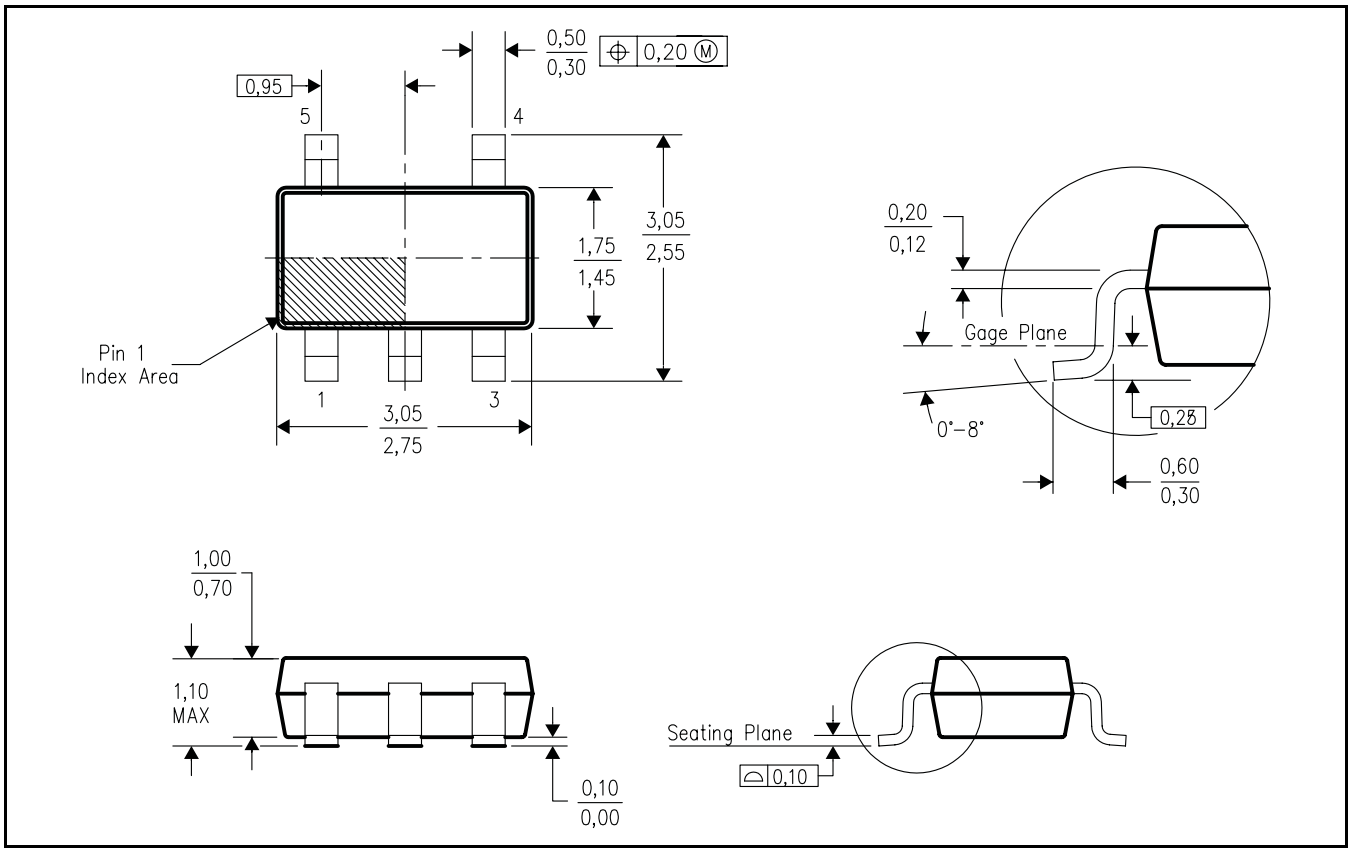
Figure 26. Recommended Land Pattern for DCK Package



(1) All linear dimensions are in millimeters.

(2) Small outline no-lead (SON) package configuration.

Figure 27. DSE Package Dimensions

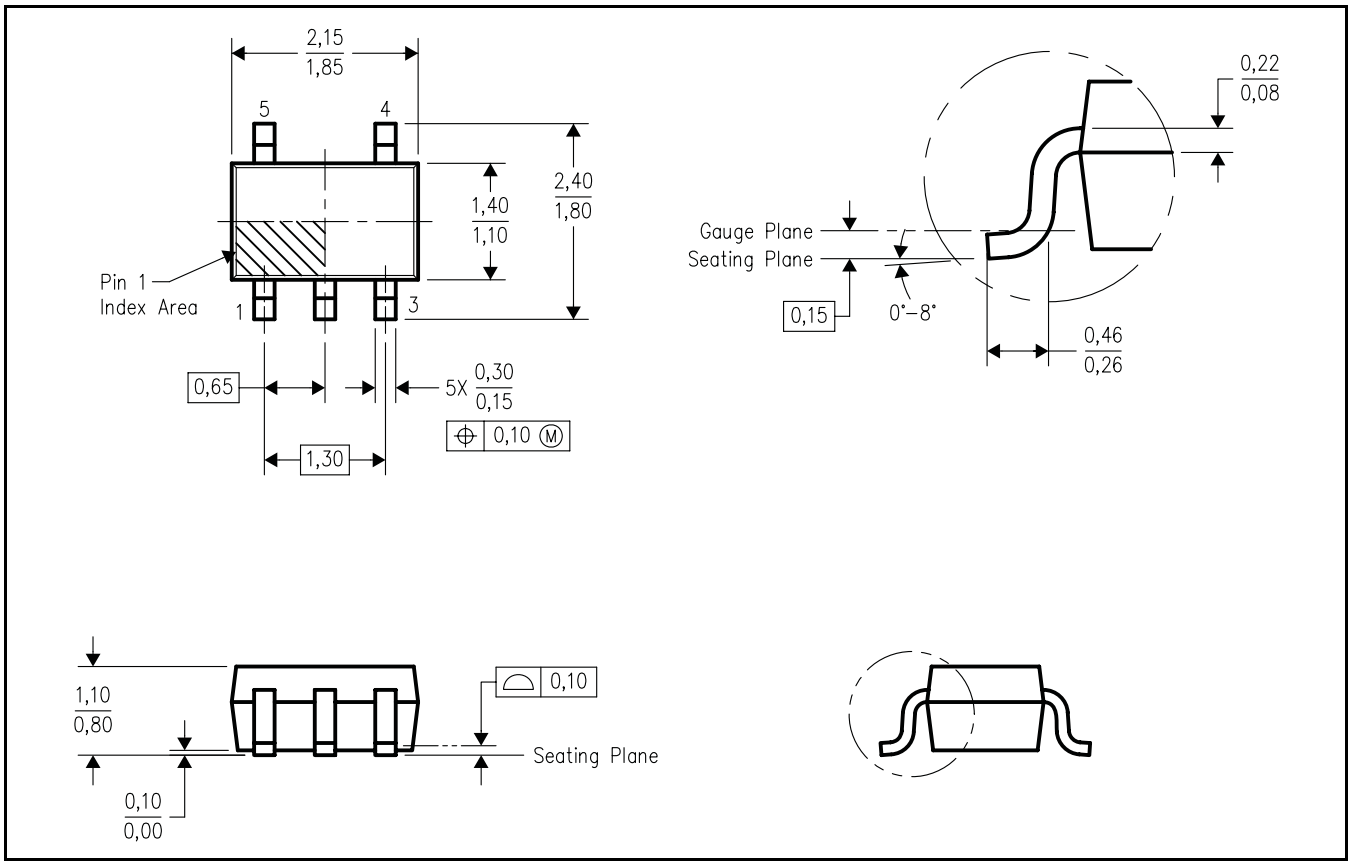


(1) All linear dimensions are in millimeters.

(2) Body dimensions do not include mold flash or protrusion.

(3) Falls within JEDEC MO-193 variation AB (pin 5).

Figure 28. DDC Package Dimensions



(1) All linear dimensions are in millimeters.

(2) Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0,15 per side.

(3) Falls within JEDEC MO-203 variation AA.

Figure 29. DCK Package Dimensions

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September, 2009) to Revision A	Page
• Changed *Very low dropout* bullet in Features list	1
• Revised SOT23-5 package name to TSOT23-5 throughout document	1
• Added TLV701xx device to document; updated references to specific devices to reflect new device availability	1
• Changed last sentence of *Description* section	1
• Deleted Revised condition statement for *Electrical Characteristics*	3
• Updated test conditions for *Line regulation* parameter	3
• Changed *Dropout voltage* parameter; added separate performance specifications and different test conditions	3
• Added new test condition and performance specification for *Ground pin current (shutdown)* parameter	3
• Changed test condition for *Enable pin current* parameter	3
• Added *Active pulldown resistance* parameter	3
• Added figure number to TLV700xx functional block diagram	4
• Added Figure 2	4
• Revised *Shutdown* section	11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLV70012DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70012DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70012DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV70012DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV70012DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70012DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70015DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70015DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70015DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV70015DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV70015DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70015DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70018DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70018DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70018DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV70018DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV70018DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70018DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70025DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV70025DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV70025DSER	PREVIEW	WSON	DSE	6	3000	TBD	Call TI	Call TI
TLV70025DSET	PREVIEW	WSON	DSE	6	250	TBD	Call TI	Call TI
TLV70028DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70028DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70028DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV70028DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS &	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
						no Sb/Br)		
TLV70028DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70028DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70029DSER	ACTIVE	WSON	DSE	6	3000	TBD	Call TI	Call TI
TLV70029DSET	ACTIVE	WSON	DSE	6	250	TBD	Call TI	Call TI
TLV70030DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70030DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70030DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV70030DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV70030DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70030DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70033DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70033DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70033DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV70033DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV70033DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70033DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV70133DSER	PREVIEW	WSON	DSE	6	3000	TBD	Call TI	Call TI
TLV70133DSET	PREVIEW	WSON	DSE	6	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF TLV70033 :

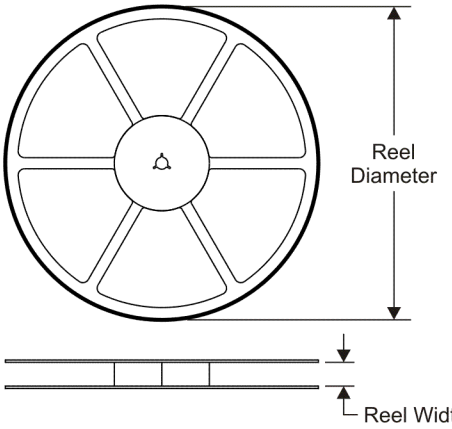
- Automotive: TLV70033-Q1

NOTE: Qualified Version Definitions:

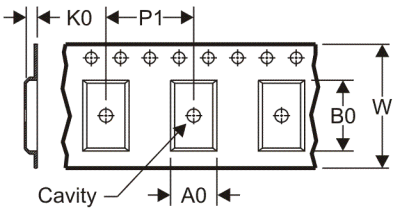
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

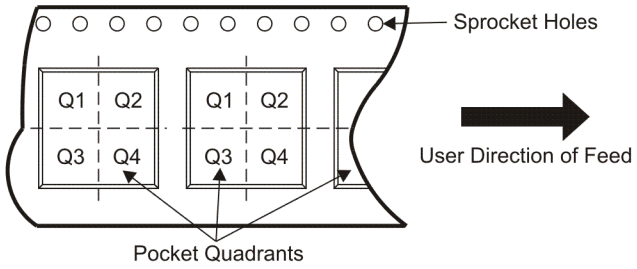


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

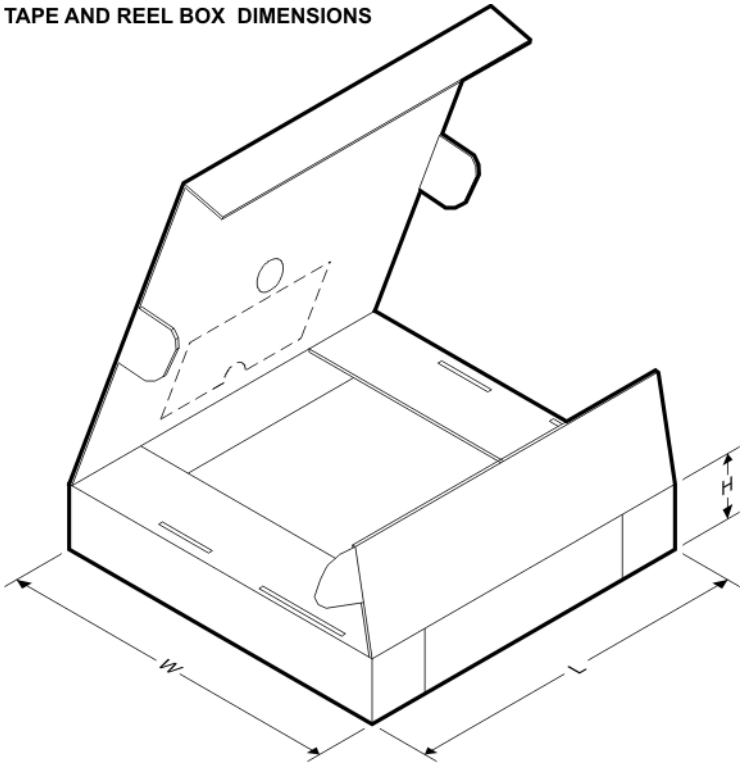


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70012DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70012DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70015DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70015DCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70015DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70015DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70015DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70015DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70018DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70018DCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70018DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70018DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70018DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70018DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70028DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70028DCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70028DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70028DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70028DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70028DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70030DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70030DCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70030DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70030DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70030DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70030DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70033DCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70033DCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV70033DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70033DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70033DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70033DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

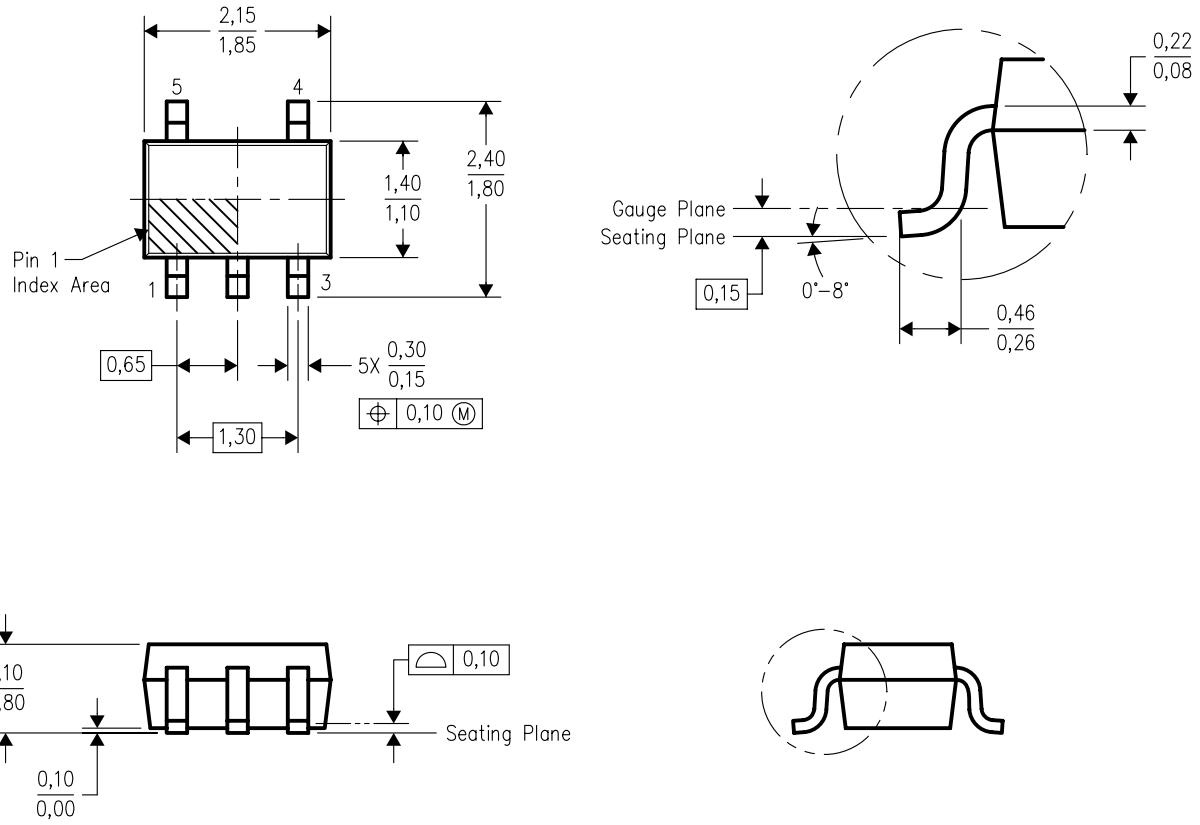


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70012DSER	WSON	DSE	6	3000	195.0	200.0	45.0
TLV70012DSET	WSON	DSE	6	250	195.0	200.0	45.0
TLV70015DCKR	SC70	DCK	5	3000	195.0	200.0	45.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70015DCKT	SC70	DCK	5	250	195.0	200.0	45.0
TLV70015DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70015DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TLV70015DSER	WSON	DSE	6	3000	195.0	200.0	45.0
TLV70015DSET	WSON	DSE	6	250	195.0	200.0	45.0
TLV70018DCKR	SC70	DCK	5	3000	195.0	200.0	45.0
TLV70018DCKT	SC70	DCK	5	250	195.0	200.0	45.0
TLV70018DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70018DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TLV70018DSER	WSON	DSE	6	3000	195.0	200.0	45.0
TLV70018DSET	WSON	DSE	6	250	195.0	200.0	45.0
TLV70028DCKR	SC70	DCK	5	3000	195.0	200.0	45.0
TLV70028DCKT	SC70	DCK	5	250	195.0	200.0	45.0
TLV70028DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70028DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TLV70028DSER	WSON	DSE	6	3000	195.0	200.0	45.0
TLV70028DSET	WSON	DSE	6	250	195.0	200.0	45.0
TLV70030DCKR	SC70	DCK	5	3000	195.0	200.0	45.0
TLV70030DCKT	SC70	DCK	5	250	195.0	200.0	45.0
TLV70030DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70030DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TLV70030DSER	WSON	DSE	6	3000	195.0	200.0	45.0
TLV70030DSET	WSON	DSE	6	250	195.0	200.0	45.0
TLV70033DCKR	SC70	DCK	5	3000	195.0	200.0	45.0
TLV70033DCKT	SC70	DCK	5	250	195.0	200.0	45.0
TLV70033DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70033DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TLV70033DSER	WSON	DSE	6	3000	195.0	200.0	45.0
TLV70033DSET	WSON	DSE	6	250	195.0	200.0	45.0

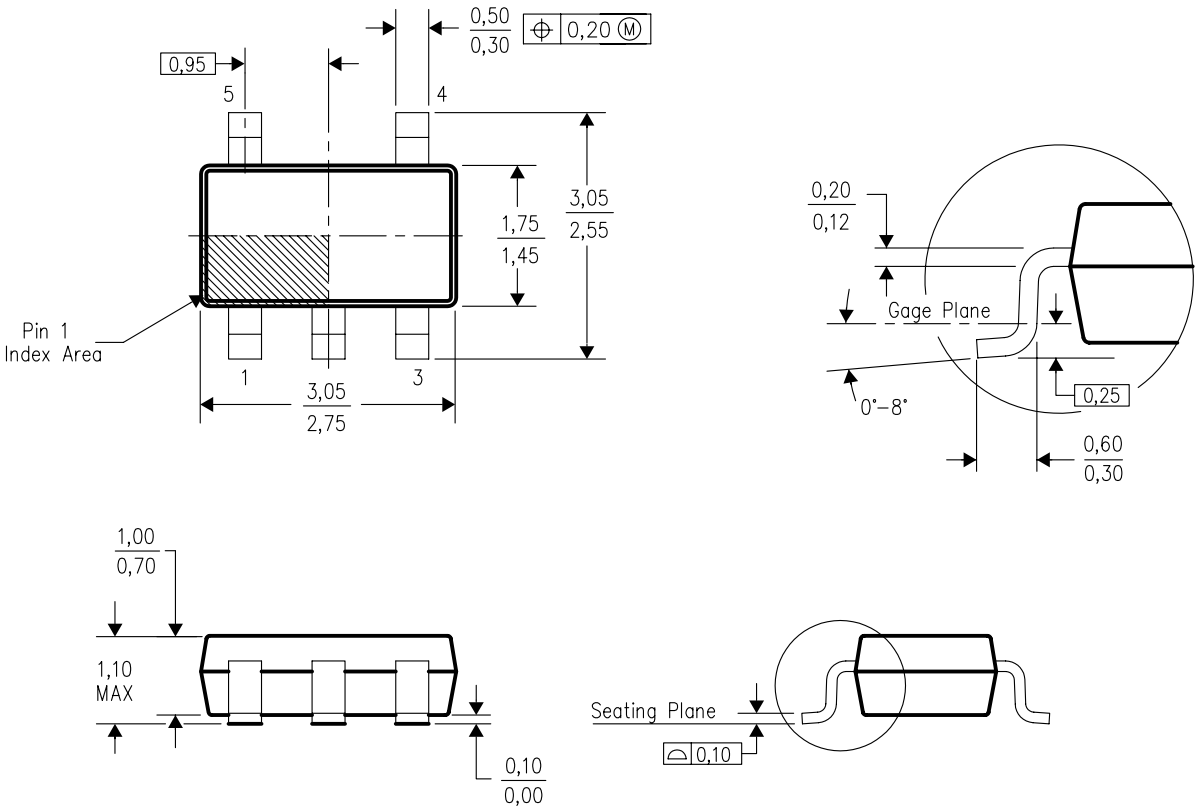
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

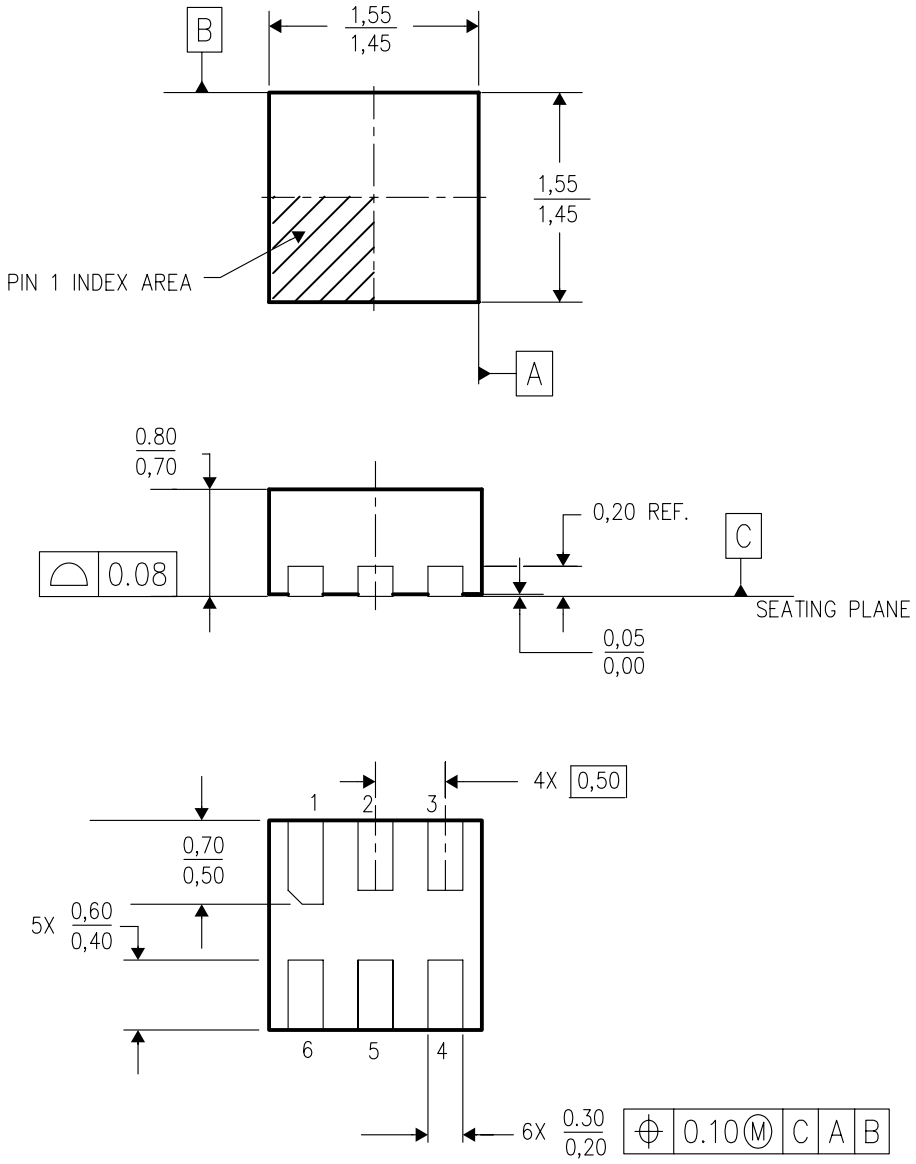
DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE



4204403–2/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE



4207810/A 03/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

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